# Refine Search

**Search Results -**

| Term | Documents |
|---|---|
| (4 AND 25).PGPB,USPT. | 18 |
| (L4 AND L25).PGPB,USPT. | 18 |

1:6F2/3Y

**Database:**
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

**Search:** L29

Refine Search

Recall Text | Clear | Interrupt

## Search History

**DATE: Friday, May 25, 2007** Purge Queries Printable Copy Create Case

| Set Name side by side | Query | Hit Count | Set Name result set |
|---|---|---|---|
| *DB=PGPB,USPT; PLUR=YES; OP=OR* | | | |
| L29 | l4 and l25 | 18 | L29 |
| L28 | l4 and l24 | 24 | L28 |
| L27 | l18 and L25 | 93 | L27 |
| L26 | l18 and L24 | 133 | L26 |
| L25 | (712/20-225)[CCLS] | 8916 | L25 |
| L24 | (712/2-300)[CCLS] | 13376 | L24 |
| *DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR* | | | |
| L23 | ("all" or every or each) near12 (nop$1 or "no" near1 operation$1) near25 (1 or 0 or one or zero$3 or set or reset$4 or mask$5) | 53 | L23 |
| L22 | ("all" or every or each) near12 (nop$1 or "no" near1 operation$1) near25 mask$5 | 0 | L22 |
| L21 | l19 not 20 | 15 | L21 |

| | | | |
|---|---|---|---|
| L20 | L19 and (vliw or very near1 (large or long) near1 instruction$1) | 13 | L20 |
| L19 | (all or plur$7 or multipl$6 or two or dual or second or every or each) near10 (nop$1) near12 (detect$3 or determin$7) | 57 | L19 |
| L18 | (nop$1) near12 (detect$3 or determin$7) | 513 | L18 |
| L17 | L16 and (vliw or very near1 (large or long) near1 instruction$1) | 8 | L17 |
| L16 | (nop$1) near12 (each or every or all) | 66 | L16 |
| L15 | L12 and (vliw or very near1 (large or long) near1 instruction$1) | 68 | L15 |
| L14 | L12 near75 (vliw or very near1 (large or long) near1 instruction$1) | 7 | L14 |
| L13 | L12 near25 (vliw or very near1 (large or long) near1 instruction$1) | 7 | L13 |
| L12 | (combin$7 or compar$6 or mask$5) near15 nop$1 | 458 | L12 |
| L11 | L10 near18 (single or final or overal$5 or sum$6 or "AND" or "ANDed" or combin$6) | 3 | L11 |
| L10 | mask$5 near10 nop$1 | 84 | L10 |
| L9 | L8 not l6 | 18 | L9 |
| L8 | ("all" or every) near12 (nop$1 or "no" near1 operation$1) and (vliw or very near1 (large or long) near1 instruction$1) | 21 | L8 |
| L7 | L4 and (vliw or very near1 (large or long) near1 instruction$1) | 5 | L7 |
| L6 | L5 and (vliw or very near1 (large or long) near1 instruction$1) | 5 | L6 |
| L5 | L4 and (nop$1 or mask$6) | 60 | L5 |
| L4 | ("all" or every or "AND" or "ANDed") near12 (nop$1 or "no" near1 operation$1) near15 ("true" or one or "1" or mask$5 or set$4 or reset$5) | 120 | L4 |
| L3 | ("all" or every) near12 (nop$1 or "no" near1 operation$1) near15 mask$5 | 0 | L3 |
| *DB=USPT; PLUR=YES; OP=OR* | | | |
| L2 | 5893143.pn. | 1 | L2 |
| L1 | 893143.pn. | 0 | L1 |

END OF SEARCH HISTORY

Results for "((nop <and> (vliw*, very <near/1> (large, long)))<in>metadata)" e-mail

Your search matched 5 of 1583645 documents.

A maximum of 100 results are displayed, 25 to a page, sorted by Relevance in Descending order.

» Search Options

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New Search

Modify Search

((nop <and> (vliw*, very <near/1> (large, long)))<in>metadata) Search

Check to search only within this results set

» Key

Display Format: Citation Citation & Abstract

| | |
|---|---|
| IEEE JNL | IEEE Journal or Magazine |
| IET JNL | IET Journal or Magazine |
| IEEE CNF | IEEE Conference Proceeding |
| IET CNF | IET Conference Proceeding |
| IEEE STD | IEEE Standard |

view selected items Select All Deselect All

1. **Hierarchical instruction encoding for VLIW digital signal processors**
Chia-Hsien Liu; Tay-Jyi Lin; Chie-Min Chao; Pi-Chen Hsiao; Li-Chun Lin; Shin-Kai Chen; Chao-We Chein-Wei Jen;
Circuits and Systems, 2005. ISCAS 2005. IEEE International Symposium on
23-26 May 2005 Page(s):3503 - 3506 Vol. 4
Digital Object Identifier 10.1109/ISCAS.2005.1465384
AbstractPlus | Full Text: PDF(696 KB) IEEE CNF
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2. **A method of speculative dual-path execution for VLIW processors**
Shimajiri, H.; Yoshida, T.;
TENCON 2004. 2004 IEEE Region 10 Conference
Volume B, 21-24 Nov. 2004 Page(s):195 - 198 Vol. 2
Digital Object Identifier 10.1109/TENCON.2004.1414565
AbstractPlus | Full Text: PDF(4841 KB) IEEE CNF
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3. **An efficient VLIW DSP architecture for baseband processing**
Tay-Jyi Lin; Chin-Chi Chang; Chen-Chia Lee; Chein-Wei Jen;
Computer Design, 2003. Proceedings. 21st International Conference on
13-15 Oct. 2003 Page(s):307 - 312
Digital Object Identifier 10.1109/ICCD.2003.1240911
AbstractPlus | Full Text: PDF(548 KB) IEEE CNF
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4. **Higher performance and lower power enhancements to VLIW architectures**
Gass, W.;
Signal Processing Systems, 2001 IEEE Workshop on
26-28 Sept. 2001 Page(s):157
Digital Object Identifier 10.1109/SIPS.2001.957342
AbstractPlus | Full Text: PDF(45 KB) IEEE CNF
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5. **A 4-way VLIW embedded multimedia processor**
Suga, A.; Sukemura, T.; Takahashi, H.; Wada, K.; Miyake, H.; Nakamura, Y.; Takebe, Y.; Azegami M.; Okano, T.; Shiota, T.; Saito, M.; Wakayama, S.; Ozawa, T.; Satoh, T.; Sakurai, A.; Katayama, T K.;
Solid-State Circuits Conference, 2000. Digest of Technical Papers. ISSCC. 2000 IEEE Internationa

7-9 Feb. 2000 Page(s):240 - 241, 461
Digital Object Identifier 10.1109/ISSCC.2000.839767